# Syllabus

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| **SN** | **21CSH-281** | **Course Name: Computer Organization & Architecture** | **L** | **T** | **P** | **S** | **C** | **CH** | **Course Type** |
| 1 | Course Coordinator: Siddharth Kumar | 3 | 0 | 0 | 0 | 3 | 3 | Core |
| **PREREQUISITE** | | 20CST212 | | | |  | | | |
| **CO-REQUISITE** | | Nil | | | |  | | | |
| **ANTI-REQUISITE** | | Nil | | | |  | | | |

* 1. **Course Objectives:**

1. The purpose of the course is to introduce principles of computer organization and the basic architectural concepts.
2. It begins with basic organization, design, and programming of a simple digital computer and introduces simple register transfer language to specify various computer operations.
3. Topics include computer arithmetic, instruction set design, microprogrammed control unit, pipelining and vector processing, memory organization and I/O systems, and multiprocessors.
4. To familiarize Students with the detailed Architectures of a Central Processing Unit.
5. Learn the different types of serial communication techniques.
   1. **Course Outcomes**

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| --- | --- |
| **CO1** | Identify and interpret the basics of instruction sets and their impact on the design, organization, and functionality of various functional units of a computer comparable to the CPU, memory organisation, I/O organization, and parallel processors. |
| **CO2** | Analysis of the design of arithmetic & logic unit and understanding of the fixed point and floating-point arithmetic operations. |
| **CO3** | Relate cost performance and design trade-offs in designing and constructing a computer processor which includes memory. |
| **CO4** | Understanding the different ways of communicating with I/O devices and standard I/O interfaces. |
| **CO5** | Implementation of control unit techniques and the concept of Pipelining. |

* 1. **Syllabus**
     1. **Theory**

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| --- | --- | --- |
| **Unit-1** | **Basic Organization of Computer** | Contact Hours:15 hours |
|  | **Revision of basics in Boolean logic and Combinational/Sequential Circuits**. | |
| **Data representation** | Signed number representation, fixed and floating-point representations, character representation. | |
| **Functional blocks of a computer** | CPU, memory, input-output subsystems, control unit. | |
| **Instruction set architecture of a CPU** | Registers, instruction execution cycle, RTL interpretation of instructions, addressing modes, instruction set. Outlining instruction sets of some common CPUs. | |
| **Computer arithmetic** | Integer addition and subtraction, ripple carry adder, carry look-ahead adder, etc. multiplication – shift-and-add, Booth multiplier, carry save multiplier, etc. Division restoring and non-restoring techniques, floating point arithmetic, IEEE 754 format. | |
| **Unit-2** | **Control Unit and Memory Organization** | Contact Hours:15 Hours |
| **CPU control unit design** | Hardwired and micro-programmed design approaches, design of a simple hypothetical CPU. | |
| **Memory system design** | Semiconductor memory technologies, memory organization | |
| **Memory organization** | Memory interleaving, concept of hierarchical memory organization, cache memory, cache size vs. block size, mapping functions, replacement algorithms, write policies. | |
| **Unit-3** | **I/O Organization and Parallel Processors** | Contact Hours: 15 Hours |
| **Peripheral devices and their characteristics** | Input-output subsystems, I/O device interface, I/O transfers – program controlled, interrupt driven and DMA, privileged and non-privileged instructions, software interrupts and exceptions. Programs and processes – role of interrupts in process state transitions, I/O device interfaces – SCII, USB | |
| **Pipelining** | Basic concepts of pipelining, throughput and speedup, pipeline hazards. | |
| **Parallel Processors** | Introduction to parallel processors, Concurrent access to memory and cache coherency. | |

**Self-study topics for Advance learners**:

* 1. **Text Books / Reference Books**

**TEXT BOOKS**

**T1:** Computer System Architecture M. M. Mano: 3rd ed., Prentice Hall of India, New Delhi, 1993.

**T2:** Computer Organization and Design: The Hardware/Software Interface, David A. Patterson and John L. Hennessy.

**T3:** Computer Organization and Embedded Systems, Carl Hamacher.

**REFERENCE BOOKS**

**R1:** Computer Architecture and Organization, John P. Hayes.

**R2:** Computer Organization and Architecture: Designing for Performance, William Stallings.

**R3:** Computer System Design and Architecture, Vincent P. Heuring and Harry F. Jordan.

* 1. **CO-PO & CO-PSO Articulation Matrix**

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| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | **PO1** | **PO2** | **PO3** | **PO4** | **PO5** | **PO6** | **PO7** | **PO8** | **PO9** | **PO10** | **PO11** | **PO12** | **PSO1** | **PSO2** | **PSO3** | **PSO4** |
| **CO1** | 3 | 2 | 2 | 1 | - | 2 | - | - | - | - | - | 3 | - | - | - | - |
| **CO2** | 3 | 3 | 3 | 1 | - | 2 | - | - | - | - | - | 3 | - | - | - | - |
| **CO3** | 3 | 3 | 3 | 2 | - | 3 | - | - | - | - | - | 3 | - | - | - | - |
| **CO4** | 3 | 2 | 2 | 2 | - | 3 | - | - | - | - | - | 3 | - | - | - | - |
| **CO5** | 3 | 2 | 2 | 2 | - | 3 | - | - | - | - | - | 3 | - | - | - | - |

**Assessment Pattern**

For the **Theory Courses**, the performance of students is evaluated as follows:

|  |  |  |
| --- | --- | --- |
| **Components** | **Continuous Internal Assessment (CAE)** | **Semester End Examination (SEE)** |
| **Marks** | 40 | 60 |
| **Total Marks** | 100 | |

Frequency for assessment tools for theory classes

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Sr. No.** | **Type of Assessment Task** | **Weightage of Actual conduct** | **Frequency of Task** | **Final Weightage of internal assessment (Prorated Marks)** |
| 1 | Assignment\* | 10 Marks for each assignment | One per unit | 10 Marks |
| 2 | Time bound Surprise Test | 12 Marks for each test | One per unit | 4 Marks |
| 3 | Quiz | 4 marks for each quiz | Two per unit | 4 Marks |
| 4 | Mid-Semester Test\*\* | 20 Marks for one MST | Two per semester | 20 Marks |
| 5 | Presentation\*\*\* | NA | As Applicable | Non-Graded Engagement Task |
| 6 | Homework | NA | One per lecture topic (of 2 questions) | Non-Graded Engagement Task |
| 7 | Discussion Forum | NA | One per chapter | Non-Graded Engagement Task |
| 8 | Attendance and Engagement Score | NA | NA | 2 Marks |

\*Every teacher should include one innovation based (Video/Simulation/LTI Based) assignment for the

students other than only essay type questions.

\*\*Mid-Semester Test to be conducted physical in examination halls. But in case the COVID

scenario extends, then it has to be conducted in Online Model via proctored examination

software.

\*\*This category may be graded in case of Seminar/Project type courses.